IN THE CLAIMS

What is claimed is:

1. A multi-layer circuit board, comprising:

at least one signal trace disposed on a dielectric layer, wherein the at least one signal trace comprises a first width that is wider than a second width; and

at least one via electrically connected to the first width of the at least one signal trace.

2. The multi-layer circuit board of claim 1 wherein the ratio of the first width to the second width is between about 2:1 and 3:1.

3. The multi-layer circuit board of claim 1 wherein the first width of at least one signal trace is located in a signal trace anti-pad region, wherein the signal trace anti-pad region extends from the center of the via to slightly past the edge of an anti-pad region.

4. The multi-layer circuit board of claim 1 wherein the second width of the at least one signal trace is located in a ground plane region, wherein the ground plane region extends from slightly past the edge of an anti-pad region to the end of the signal trace opposite the first width of the signal trace.

5. The multi-layer circuit board of claim 1 wherein the signal trace further comprises a via pad.

6. The multi-layer circuit board of claim 1 wherein the first width of the at least one signal trace is not substantially disposed over a ground plane.

7. The multi-layer circuit board of claim 1 wherein an impedance discontinuity between the signal trace and a component electrically connected to the via is lowered from above 5 ohms to less than 1 ohm.

8. A test structure, comprising:

at least one signal trace disposed on a dielectric layer, wherein the at least one signal trace comprises a first width that is wider than a second width;

a via connected to the first width of the at least one signal trace; and

a component electrically attached to the via, wherein an impedance discontinuity between the at least one signal trace and the component is lowered.

9. The test structure of claim 8 wherein the ratio of the first width to the second width is between about 2:1 and 3:1.

10. The test structure of claim 8, wherein the first width is located in a signal trace anti-pad region, and the second width is located in a ground plane region.

11. The test structure of claim 8 wherein the at least one signal trace is not substantially disposed over an underlying ground plane in the signal trace anti-pad region.

12. The test structure of claim 8 wherein the component is one of a SMA, BNC or SIP connector.

13. The test structure of claim 8 wherein the component is one of a socket, a microprocessor, or a circuit component.

14. The test structure of claim 8 wherein the impedance discontinuity between the at least one signal trace and the component is lowered from above 5 ohms to below 1 ohm.

15. The test structure of claim 8, wherein the component is adapted for receiving a signal.

16. The test structure of claim 8, wherein the signal is launched through a prober and a signal output is coupled to the component.

17. The test structure of claim 15, wherein the signal has a frequency of above about 5 Gigahertz.

18. A test system, comprising:

a TDR prober including a signal output and a signal ground;

at least one ground pad disposed on a dielectric layer, wherein the ground pad is coupled to the signal ground;

at least one signal trace disposed on the dielectric layer, wherein the at least one signal trace comprises a first width that is wider than a second width; and

a component electrically connected to the first width of the at least one signal trace, wherein the component is coupled to the signal output.

19. The test system of claim 18 wherein the ratio of the first width to the second width is between about 2:1 and 3:1.

20. The test system of claim 18 wherein the component is a SMA connector.

21. The test system of claim 18 wherein the TDR prober comprises a TDR probing system.

22. The test system of claim 18 wherein an impedance discontinuity between the signal trace and the component is lowered from above 5 ohms to less than 1 ohm.

23. A method of forming a test structure, comprising:

forming a signal trace on a dielectric layer, wherein the signal trace comprises a first width that is wider than a second width;

electrically connecting a via to the first width of the signal trace; and

electrically connecting a component to the via, wherein the impedance discontinuity between the signal trace and the component is lowered.

24. The method of claim 23 wherein forming the signal trace comprises forming the first width of the signal trace to be wider than the second width by a ratio of between about 2:1 to about 3:1.

25. The method of claim 23 wherein electrically connecting the component to the via comprises lowering the impedance discontinuity between the signal trace and the component from above 5 ohms to below 1 ohm.